Amendments to the Specification

Replace the paragraph beginning at page 4, line 1, with the following amended paragraph:

--One way of applying the DC voltage is to connect the DC voltage source to an electrode of the capacitor through a resistor. Often, a DC blocking capacitor must be used in the RF signal path so as to provide an RF ground for example, to the ~~f-e~~ FE capacitor without shorting out the ~~dc~~ DC bias applied. The DC blocking capacitor invariably introduces added loss into the RF signal. This increased loss results in a lower signal to noise ratio for receive applications, which results in dropped communications, and increased power consumption in transmit applications, among other things. Additionally, the resistor and the DC blocking capacitor add to the cost, size and complexity of the device that the capacitor is used in. Thus, this method of applying the variable DC electric filed to the FE material is not an optimal solution.--

Replace the paragraph beginning at page 4, line 17, with the following amended paragraph:

--While planar ~~f-e~~ FE capacitors are relatively simple to fabricate, they require a larger DC bias voltage to tune, as the gap dimensions are necessarily large (typically greater than or equal to 2.0 microns) due to conventional patterning constraints. Overlay ~~f-e~~ FE capacitors, alternatively, can be tuned with a minimum DC voltage, as the plate separation can be made quite small (about 0.1 micron ~~f-e~~ FE film thickness is possible and greater than about 0.25 microns is typical). Thus, the required DC bias field strength can be a factor of 20 to 40 times smaller for an overlay capacitor than for a gap capacitor. Furthermore, most all of the ~~dc~~ DC bias field is constrained within the ~~f-e~~ FE film in an overlay capacitor. This is not true in a gap or interdigital capacitor, where a significant portion of the ~~dc~~ DC bias field is located outside of the ~~f-e~~ FE film.--

Replace the paragraph beginning at page 5, line 9, with the following amended paragraph:

--One significant problem with overlay capacitors is that they are more difficult to fabricate than gap capacitors, as they are multi-layer structures. They typically need a common bottom electrode on which the desired ~~f-e~~ FE thin film is deposited. Ideally the desired metals for the bottom electrodes are typically the low loss noble metals like gold, silver or preferably copper. The deposition requirements for most ~~f-e~~ FE films, however, would cause the unacceptable formation of metal oxides. To prevent unwanted oxidation, the deposition of a high refractory metal, such as platinum

as a cap, or covering, layer is needed, which adds an extra mask or layer as well as increases cost. Additionally, the bottom layer metal thickness should be increased to greater than about 2.0 skin depths, to minimize the metal loss in the bottom electrode.--

Replace the paragraph beginning at page 6, line 1, with the following amended paragraph:
--Rather than relying on overlay capacitors, a compromise solution is to introduce a pair of bias electrodes into the vicinity of the gap of a planar capacitor. One version would pattern one bias electrode in the gap itself and place the other electrode between the substrate and the ~~f-e~~ FE layer. The variable DC electric field is applied to the FE material by putting bias electrodes in the form of doped silicon on both sides of the FE material. Thus, a first doped silicon layer is formed on the substrate. A FE layer is formed on the first doped silicon layer. The capacitor electrodes are formed on the FE layer. A second doped silicon layer is formed inside the gap region of the capacitor. The bias voltage is applied to the second doped silicon layer and the first doped silicon layer is grounded, or vice versa. This approach is not preferred, as it requires the presence of two bias electrodes, one above and one below the ~~f-e~~ FE layer as well as the presence of a bias electrode between the two ~~rf~~ RF electrodes in the gap capacitor.--

Replace the paragraph beginning at page 9, line 22, with the following amended paragraph:
--In other words, only one bias electrode is introduced, as an underlay, beneath the ~~f-e~~ FE film layer deposited on the base substrate. In this configuration, the ~~rf~~ RF electrodes provide the ~~dc~~ DC return paths for the ~~dc~~ DC bias signal. In this realization there is no need for an external ~~dc~~ DC blocking capacitor as the ~~dc~~ DC bias introduced in this manner is inherently isolated from the rest of the circuit. A further advantage of this arrangement is that one need not increase the gap in the gap capacitor to accommodate the presence of a two layer bias electrode structure. Thus the most compact gap capacitor realization can be obtained in this manner.--

Replace the paragraph beginning at page 10, line 11, with the following amended paragraph:
--The gap capacitor will now be described with reference to Fig. 1. Fig. 1 is a side view of a tunable FE capacitor 10. A substrate 12 is shown. The substrate 12 is typically a low loss ceramic material such as magnesium oxide, sapphire, or some other such similar material on which the desired ~~f-e~~ FE

film can be deposited, preferably without the need for an adhesion or buffer layer. The substrate can also be a more lossy material like silicon dioxide, alumina or a printed circuit board material such as the well known material, FR4 as long as one can tolerate the added loss arising from its use, along with the added cost and complexity of using one or more buffer layers or an adhesion layer that may be necessary with these substrates.--

Replace the paragraph beginning at page 11, line 1, with the following amended paragraph:
--Formed on the substrate 12 is a bias electrode 14. The bias electrode 14 is preferably doped silicon, as it can have a much lower conductivity than any metal, and its conductivity can be controlled by doping. Alternatively, the bias electrode 14 can be a metal such as gold, silver, platinum or copper. Over the bias electrode 14 is a FE layer 16. The FE layer 16 provides the tunability to the capacitor. Over the FE layer 16 are the capacitor electrodes 21 and 24. The capacitor is part of a RF signal path. The capacitor electrodes 21 and 24 define a space between the electrodes called a gap 47. The gap 47 is defined by the electrodes. The gap 47 is shown as a dotted line. The dotted line is separated somewhat from the solid line defining the capacitor electrodes 21 and 24. This is for the sake of distinguishing between the lines defining the gap 47 and the electrodes 21 and 24, not to indicate that there is any space between the gap 47 and the electrodes 21 and 24. The gap 47 and the electrodes 21 and 24 are coterminous.--

Replace the paragraph beginning at page 11, line 20, with the following amended paragraph:
--The gap capacitor will now be described with reference to Fig. 2A. Fig. 2A is a top view of the gap capacitor. A first capacitor electrode 43 and a second capacitor electrode 45 form a capacitor gap 47. In one implementation, the second electrode 45 is positioned within 3.0 microns of the first electrode 43. A ferro-electric material 53 lies preferably underneath the first and second capacitor electrodes 43 and 45. The ferro-electric material 53 could alternatively lie over the top of the first and second capacitor electrodes 43 and 45 assuming the proper precautions are taken to prevent the oxidation or melting of the metal traces 43 and 45 during the deposition of the ~~f-e~~ FE film on top of the electrodes. Due to these limitations, the ~~f-e~~ FE film will almost always be under the ~~rf~~ RF metal contacts, 43 and 45. In one implementation, the FE material 53 comprises barium strontium titanate and is formed in a layer having a thickness equal to about one micron.--

Replace the paragraph beginning at page 17, line 11, with the following amended parapgrah:

--The bias electrode 55 is electrically thin, preferably less than about 0.01 microns so that it is less than about 0.1 skin depths. The added ~~rf~~ RF loss arising from the presence of the bias electrode is minimal and its effect is offset by the advantage gained in fabrication and improved tuning. In one implementation, the RF signal has a frequency equal to about 2.0 GHz, and the bias electrode 55 causes a field attenuation of about 0.28 percent in the RF signal.--